CLAIMS

1. A semiconductor device having a MIS-type field effect transistor comprising:

a concave formed in at least a semiconductor substrate;

a channel region formed on a bottom surface of said concave;

source/drain extension regions connected to both ends of said channel region and formed on the bottom surface of said concave; and

source/drain regions being close to or adjacent to side surfaces of said concave, formed along a surface of said semiconductor substrate in a direction of depth, and connected to said source/drain extension regions,

characterized in that side surfaces of said concave on a source/drain side constitute a rounded surface.

2. A semiconductor device according to claim 1, wherein said concave is constituted by a trench formed from the surface of said semiconductor substrate in the direction of depth.

3. A semiconductor device according to claim 1, wherein a position where an impurity concentration of said source/drain regions in the direction of depth is maximum almost coincides with a position where an impurity concentration of said source/drain extension regions in the direction of depth is maximum at a

connecting portion between said source/drain regions and said source/drain extension regions.

4. A semiconductor device according to claim 1, wherein a taper angle set to upwardly increase the opening portion is given to said concave.

5. A semiconductor device according to claim 1, wherein ion implantation for threshold voltage control of said MIS-type field effect transistor is performed to only the bottom surface of said concave.

6. A semiconductor device according to claim 1, further comprising a gate formed on the bottom surface of said concave through a gate insulating film, and gate sidewall spacers consisting of an insulator formed on side surfaces of said gate, characterized in that said gate sidewall spacers are formed to partially cover the side surfaces of said concave extending on at least the source/drain side of said gate.

7. A semiconductor device according to claim 2, wherein a position where an impurity concentration of said source/drain regions in the direction of depth is maximum almost coincides with a position where an impurity concentration of said source/drain extension regions in the direction of depth is maximum at a connecting portion between said source/drain regions and said source/drain extension regions.

8. A semiconductor device according to claim 6, wherein said gate sidewall spacers are formed to

entirely cover the side surfaces of said concave extending on at least the source/drain side of said gate.

9. A semiconductor device comprising:

a concave constituted by a trench formed in a semiconductor substrate;

a channel region formed on a bottom surface of said concave;

source/drain extension regions connected to both ends of said channel region and formed on the bottom surface of said concave; and

source/drain regions formed on a surface of said semiconductor substrate being close to or adjacent to side surfaces of said concave and connected to said source/drain extension regions,

characterized in that said concave comprises a MIS-type field effect transistor having side surfaces on a source/drain side constituting a rounded surface.

10. A semiconductor device according to claim 9, wherein a position where an impurity concentration of said source/drain regions in the direction of depth is maximum almost coincides with a position where an impurity concentration of said source/drain extension regions in the direction of depth is maximum at a connecting portion between said source/drain regions and said source/drain extension regions.

11. A semiconductor device according to claim 9,

wherein a taper angle set to upwardly increase the opening portion is given to said concave.

12. A semiconductor device according to claim 9, wherein ion implantation for threshold voltage control of said MIS-type field effect transistor is performed to only the bottom surface of said concave.

13. A semiconductor device according to claim 9, further comprising a gate formed on the bottom surface of said concave through a gate insulating film, and gate sidewall spacers consisting of an insulator formed on side surfaces of said gate, characterized in that said gate sidewall spacers are formed to partially cover the side surfaces of said concave extending on at least the source/drain side of said gate.

14. A semiconductor device according to claim 9, wherein said gate sidewall spacers are formed to entirely cover the side surfaces of said concave extending on at least the source/drain side of said gate.

15. A method of manufacturing a semiconductor device comprising the steps of:

forming an etching mask constituted by a first insulating film having an opening portion including a gate forming portion and source/drain extension regions forming portion on a semiconductor substrate;

forming a trench in said semiconductor substrate in correspondence with the opening portion of said

etching mask;

forming a gate insulating film constituted by a second insulating film on an inner surface of said trench;

forming a gate material film on said second insulating film;

patterning said gate material film to form a gate on a central portion between both sides of said trench on a source/drain side through said second insulating film;

implanting impurity ions into at least a bottom surface of said trench by using said gate as a mask to form source/drain extension regions;

forming a third insulating film to cover a surface of said semiconductor substrate subjected to the steps;

forming gate sidewall spacers constituted by said third insulating film by using anisotropic etching to cover the inner surface of the trench extending on the source/drain side of said gate; and

implanting impurity ions into the source/drain regions by using said gate having the gate sidewall spacers as a mask to form a MIS-type field effect transistor having source/drain regions being close to or adjacent to side surfaces of the trench of said semiconductor substrate and connected to the source/drain extension regions on the bottom surface of said trench.

16. A method of manufacturing a semiconductor device according to claim 15, wherein said trench is formed by isotropic etching such that the side surfaces of said trench on the source/drain side constitute a rounded surface.

17. A method of manufacturing a semiconductor device according to claim 15, wherein ion implantation for threshold voltage control of said MIS-type field effect transistor is performed to only the bottom surface of said trench.

18. A method of manufacturing a semiconductor device according to claim 15, wherein said first, second, and third insulating films are an SiO_2 film formed by an LPCVD method using TEOS, an SiO_2 film formed by thermal oxidation of silicon, and an SiN film formed by a CVD method, respectively.

19. A method of manufacturing a semiconductor device according to claim 15, wherein said first insulating film is formed to be stacked on a thermal oxidation film formed as a buffer layer on said semiconductor substrate.

20. A method of manufacturing a semiconductor device according to claim 15, further comprising the steps of, after a silicide film of high melting point metal is formed on a silicon surface exposed to the source/drain regions and upper surfaces of said gate consisting of polysilicon by forming a high melting

point metal film to cover the surface of said semiconductor substrate and performing heat treatment, removing said high melting point metal film remaining on the gate sidewall spacers.

21. A method of manufacturing a semiconductor device comprising the steps of:

forming an etching mask constituted by a first insulating film having an opening portion including a gate forming portion and source/drain extension regions forming portion on a semiconductor substrate;

forming a trench in said semiconductor substrate in correspondence with the opening portion of said etching mask;

forming a gate insulating film constituted by a second insulating film on an inner surface of said trench;

forming a gate material film to cover the surface of said semiconductor substrate subjected to the above steps;

further forming a third insulating film on said gate material film;

etching-back the upper surfaces of said third insulating film and said gate material film to form a gate forming etching mask constituted by said third insulating film buried in said gate material film on a central portion between both sides of the mask opening portion on the source/drain side; and

anisotropically etching said gate material film by using said third insulating film buried in said gate material film as a mask to process said gate, thereby forming a MIS-type field effect transistor having a self-aligned gate formed on a central portion between both sides of said trench on the source/drain side.

22. A method of manufacturing a semiconductor device according to claim 21, wherein when a gate length of said MIS-type field effect transistor is represented by L, a length of the opening portion, in a direction of the gate length, of the opening portion of the etching mask constituted by said first insulating film is represented by L_W, and the thickness of said gate material film is represented by d, a relationship $L \leqq L_W - 2d$ is satisfied.

23. A method of manufacturing a semiconductor device according to claim 21, wherein said trench is formed by isotropic etching such that the side surfaces of said trench on the source/drain side constitute a rounded surface.

24. A method of manufacturing a semiconductor device according to claim 21, wherein ion implantation for threshold voltage control of said MIS-type field effect transistor is performed to only the bottom surface of said trench.

25. A method of manufacturing a semiconductor device according to claim 21, wherein said first,

second, and third insulating films are an SiO_2 film formed by an LPCVD method using TEOS, an SiO_2 film formed by thermal oxidation of silicon, and an SiN film formed by a CVD method, respectively.

26. A method of manufacturing a semiconductor device according to claim 21, wherein said first insulating film is formed to be stacked on a thermal oxidation film formed as a buffer layer on said semiconductor substrate.

27. A method of manufacturing a semiconductor device according to claim 21, further comprising the steps of:

implanting impurity ions into at least the bottom surface of said trench by using said gate as a mask to form source/drain extension regions;

forming a fourth insulating film to cover the surface of said semiconductor substrate subjected to the steps;

forming gate sidewall spacers constituted by said fourth insulating film by using anisotropic etching to cover the inner surface of said trench extending on the source/drain side of said gate; and

implanting impurity ions into the source/drain regions by using said gate having the gate sidewall spacers as a mask to form source/drain regions being close to or adjacent to side surfaces of said trench of said semiconductor substrate and connected to the

source/drain extension regions on the bottom surface of said trench.

28. A method of manufacturing a semiconductor device comprising:

forming an etching mask constituted by a first insulating film having an opening portion including a gate forming portion and source/drain extension regions forming portion on a semiconductor substrate;

forming a trench in said semiconductor substrate in correspondence with the opening portion of said etching mask;

forming a gate insulating film constituted by a second insulating film on an inner surface of said trench;

forming a third insulating film to cover the surface of said semiconductor substrate subjected to the above steps;

forming sidewall spacers constituted by said third insulating film by using anisotropic etching on side surfaces of the mask opening on a source/drain sides respectively;

forming a gate material film to cover the surface of said semiconductor substrate subjected to the above steps;

etching-back the upper surfaces of said third insulating film and said gate material film to form a gate constituted by said gate material film buried

between the sidewall spacers on a central portion between both sides of the mask opening portion on the source/drain side; and

selectively removing said first and third insulating films to form a MIS-type field effect transistor having a self-aligned gate formed on a central portion between both sides of said trench on the source/drain side.

29. A method of manufacturing a semiconductor device according to claim 28, wherein said trench is formed by isotropic etching such that the side surfaces of said trench on the source/drain side constitute a rounded surface.

30. A method of manufacturing a semiconductor device according to claim 28, wherein ion implantation for threshold voltage control of said MIS-type field effect transistor is performed to only the bottom surface of said trench.

31. A method of manufacturing a semiconductor device according to claim 28, wherein said first, second, and third insulating films are an SiO_2 film formed by an LPCVD method using TEOS, an SiO_2 film formed by thermal oxidation of silicon, and an SiN film formed by a CVD method, respectively.

32. A method of manufacturing a semiconductor device according to claim 28, wherein said first insulating film is formed to be stacked on a thermal

oxidation film formed as a buffer layer on said semiconductor substrate.

33. A method of manufacturing a semiconductor device according to claim 28, further comprising the steps of:

implanting impurity ions into at least the bottom surface of said trench by using said gate as a mask to form source/drain extension regions;

forming a fourth insulating film to cover the surface of said semiconductor substrate subjected to the steps;

forming gate sidewall spacers constituted by said fourth insulating film by using anisotropic etching to cover the inner surface of said trench extending on the source/drain side of said gate; and

implanting impurity ions into the source/drain regions by using said gate having the gate sidewall spacers as a mask to form source/drain regions being close to or adjacent to side surfaces of said trench of said semiconductor substrate and connected to the source/drain extension regions on the bottom surface of said trench.

34. A method of manufacturing a semiconductor device according to claim 33, further comprising the step of, after a silicide film of high melting point metal is formed on a silicon surface exposed to the source/drain regions and upper surfaces of said gate

consisting of polysilicon by forming a high melting point metal film to cover the surface of said semiconductor substrate and performing heat treatment, removing said high melting point metal film remaining on the gate sidewall spacers.